Optical Holographic Computer

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March 23rd, 2016:

A MAX11300 EVAL board was purchased, as well as power supply from DigiKey on the night of Wednesday.

This board features 20 simultaneous 12-bit switchable ADC and DAC controllers running at 25 mA draw at most, and runs at 20 MHz for the internal clock. It comes with software for interfacing with the computer, and has a simple programmable switching style.

It is intended to be used with 20 simultaneously switchable two dimensional active feedback resonating optical chambers, which may be attached to each other along fiber optic cables or laid flat faced against one another.

I have found difficulty finding:

1.) An active liquid crystal disc for switching of the light field.

2.) A positron-electron switchable film for the same purpose.

3.) Single strand large aperture fiber optic cable for cheap.

It is intended to be used as a series of universal gates of simple harmonic oscillator variety; as it was found that the device that I created embodies these properties in at least two dimensions with intensity as the third dimension of attenuation and gain upon the surface.

Programming of the device is intended to be controlled with the MAX11300 EVAL software or accomplished over serial input and output with an algorithm that can be compiled into something analogous to assembly, rendering the program into a primitive algorithm for which the natural evolution of the light performs a virtually instantaneous operation of calculation.

With 20 of these acrylic discs mated with re-routable fiber optic cables in a modular style, grouped into four or two separably, it is expected a universal gate structure can be built for computational purposes.

Some remaining notes are that it may be difficult to work with this device, but that once it is set up it will demonstrate the properties of an optical quantum computer; for the individual surfaces interfaced with the gain- feedback loop as designed before for the crystal/light emitting diode/photodiode touch surface. Nonlinearity needs to be taken advantage of instead of discarded, for this takes place within the fiber optics and in the acrylic discs.

There are complications with interfacing the optical fibers to perfectly mate to the discs, and with the simultaneous feedback to establish a persistent state. In addition, the signal must be amplified with operational amplifiers and laser diodes need to be purchased for signal acquisition and production.

This will require a complete re-thinking of what a computer is capable of and how to construct one, and for the most part it is nontrivial. The modular design should afford some flexibility, but as to how to address the space and produce operators of a general kind will require some thought and work.

In the end one can envisage using the massive parallelization with pulse width modulation and modular arithmetic to perform simple operations such as factoring and generalized computation with an appropriate *language* for the sake of interfacing to the computer.

1.) The problem with attaching the fiber optical cables to the acrylic discs can be remedied by trimming them to half their diameter, running them completely around the disc, and then inserting a small wedge like glass with refractive index of that of the center of the fiber optic cable in between the connections.

2.) The problem with mating the acrylic discs to one another can be remedied by choosing widths of the acrylic discs which are larger than that of the fiber optic cable, and they can then be glued to each other easily, although it may take groups of three to accomplish switching, in which case we do not need the positron electron film nor the liquid crystal discs.

3.) There will need to be twenty separately addressable operational amplifier designs as per the design with the existing prototype simple harmonic oscillator light cavity for touch reception and measurement, for independent feedback mechanisms for each disc in the stack, and these can be ran to individual laser diodes and laser photodiodes.

P1.) There needs to be a way to control phase and amplitude of the sent and received signals from the discs, for the sake of signal comparison as well as phase and gain measurement, which may be accomplished in software with the DAC and ADC, but is not robust enough without this.

P2.) There needs to be a way to match the impedance of the light field within the external device circuitry as per the old design in which photodiodes and light emitting diodes were used. Additionally, some variety of heterodyning needs to be implemented so that the carrier wave can be modulated. This may be controlled with the pulse width modulation of the ADC and DAC.

Overall what one seeks is a programmable interface for general computation with a minimal number of gates, and what needs to be innovated is a type of *language*.

Given there are 20 ADC's and DAC's, it would be possible in groups of three to have 6 gates of three fold design, and two gates for input and output and store and read, as well as to operate on the quantum optical bits.

March 26th, 2016:

The design for the operators will be one generalized universal operator as well as set union and intersection on irrational or rational numbers in a non commutative space for what are quantum bits, or analog bits of higher dimensional construction. It should be realizable to produce reducibility of the numbers from input to output through several gates.

These operators as well as the union and intersection are provided by the mathematics paper that I wrote on closed, open, true and false, and produce a non-commutative operation that reduces to outputs of open, closed, true or false. The basic sequences need to be within two channels.

It has additionally been realized that it is possible to produce switching and light wave isolation with groups of three wafers and hence switching, but because of direct mode coupling it is not possible to realize this switching with individual sets of two wafers.

As for phase and amplitude control, the ADC and DAC are sufficient for these purposes as signal generators, and should provide one with (if it is truly parallel information) the setting of the states and their readout in the real domain, while the 'processing' can take place within the 'complex' space.

It has been realized a balance can be struck between the complexity of the interconnects for naturalized operators of a generalized form and the separate algorithm computer side.

March 27th, 2016:

The device set up in six gates of transistor like arrangement resolves uniquely to the six anharmonic ratios of the elliptic functions and preserves the cross ratio. In this sense the device acts like a generalized Moebius transformation. The functions are clearly rational ratios of the Weierstrass P function with common zeros and poles, for a signal of finite domain.

In addition, the code as instanced in the paper I wrote on mathematics can be used to implement a sequence of Open, Closed, True, and False, and there needs to be two inputs and two outputs for sequences. The operators are

in the space and there are at least 64. The polynumerous types paper with rings should be sufficient to evaluate any program.

In this sense some of the problems are resolved, and it is based on a continuum for true and false around a circle without center, for two perpendicular directions of truth and falsity on a Cartesian chart without center. The information is intended to be encoded in bytes, and will operate upon a 64 value basis, with 64 squared or 4096 bit layer depth.

The device, as it has been discovered is expanded in dimension by the number of parallel gates, and they are each two dimensional with depth information. Hence there are 2^6=64 dimensions to the quantum bits, and these should admit 64 parallel operations. This leaves a remainder of two gates for input and output and error and checksum.

There needs to be some T junctions for the optical fibers for their direct and indirect connections. It has been discovered that the heterodyning and impedance matching can be accommodated by gyrators, and this is sufficient for these properties for the carrier wave and the normal wave in the optical fiber.

March 28th, 2016:

For a while I was confused about the nature of the base ground state, but now I have figured out that it is possible to produce this with wave shaping in the pulse width modulation domain for the DAC and ADC for the ground states of these devices in parallel.

I have also uncovered that the parallel streams are additive in the dimension and multiplicative in the group of operations and binary bit layer depth. There is a missing factor of two as I intend to work with two inputs and two outputs, and bit layer depth of four (4) for the base modular group of signs; with the remainder of six (6) gates and two (2) control gates; this admits bytes.

There are fewer problems than I anticipated, and it looks to be productive for work at a later point in time. The anharmonic ratios are of number six (6), so it should be possible to work with 2^6=64 base operations on Weierstrass elliptic functions preserving the cross ratio.

The final trick is to accomplish a closed form computation that makes use of the same space for the switching of the references, but as for producing a primitive form of computer it should be requisite for my tasks.

Finally as 64x64=4096 which is the same bit layer depth of the ADC and DAC, the parallel operation and serial operation should in some sense be identifiable. I anticipate good things with this instrument, but it will require

work, and a great deal of mathematical theory and modeling. This device must meet the ultimatum of simplicity in design.

I am still making up my mind about various attributes of the device; and indeed it will be expensive, but I have the ability and innovativeness and imagination to produce something simple, although I may need a FPGA controller of some kind to tailor the operations.

Remaining Questions:

1.) How do we identify the anharmonic ratios with their transformations (and therefore operations) of the states in the individual and larger spaces?

2.) What will be the topology of the interconnections in the configuration space of the optical fibers and its dimensional constraints?

3.) How precisely do we operate on the information in the eigenbasis for the sake of reading in a program and reading out the result?

4.) How much information can we preserve and what are the conditions for a completed operation or one which does not terminate?

5.) How precisely do we match the impedance condition on the waves and under what bandwidth conditions will it be representative of the information?

It has been realized that the elliptic functions do not modify the eigenbasis in such a manner that it is no longer a quantum simple harmonic oscillator. Additionally, the 25 mA driving current limit may be sufficient for a typical laser diode/photodiode, and some configurations of these photodiode/light emitting laser diodes come in the same package. This simplifies the design.

March 29th, 2016:

The given device of the touch screen advances by a phase of pi through the measurement process when signals are sent in, and as a given the space is non-commutative in the raising and lowering operators, hence this admits the operation on the quantum bits within the space by the setting and reception of signals. Although, there is remaining work to be done on the active input/output feedback and differential set/read of the quantum bits.

As a result; the setting and receiving of the signals in input and output correspond to the frequency DAC and ADC read cycles and settings.

April 5th, 2016:

Certain limitations of the prior design implementation of the device in its current crystal and light emitting diode / photodiode design, with the external device circuitry have made it apparent that there needs to be an entirely new method of implementation, and this has set back the date for the creation of an optical holographic computer. But for now, the transistor like properties of the single current design implementation can and will be characterized fully.

As for the optical holographic computer, it has become apparent that what needs to be done is to innovate a manner of implementing it as a learning neural network, with re-routable signal managing, and that this can be accomplished with a programmable flash FPGA, which can manage at high efficiency and speed the signal re- routing dynamically.

This makes a more generalized form of the given computer, with some nature of pattern recognition and pattern processing. No lesser is the avenue of using modular arithmetic and pulse width modulation for the signals to the device. As a consequence of the direct current out to the laser diodes the device design is vastly simpler.

Finally, it has been realized that it may indeed be possible to implement a comparator with two of the optical cavities so mated as transistors, in which case we can pass bytes as instructions.

April 13th, 2016:

It is clear the FPGA needs to go between the ADC/DAC and the optical components, for the sake of measurement, read, and send cycles.

April 18th, 2016:

After recent inquiry into the device properties and measurement properties of the current design implementation it has been determined that due to the properties of the variational principle; or simply that of the continuity condition on the boundary, that there exists but one minimum and one maximum on the exterior boundary, and hence there is but one maximum and one minimum in the domain.

As a consequence the holographic principle is not fully realized, or it is an inherent limitation of the device that only singular presses can be determined; although retaining the Gaussian characteristic. This places a strict limitation on the realization of full information capacity of the device to be created in the optical computer.

For a while it was speculated that due to this property of only identifying singular presses that what I had invented was merely a spin 1 qubit, but instead it has been determined owing due to the expansion in the Gaussian series with Hermite polynomials and the light cavity modes in their relationship to this expansion that it is indeed a simple harmonic oscillator.

Therefore however we are to proceed we are constrained by the limitation of radial and azimuthal coordinate and depth.

April 20th, 2016:

It has been determined by comparing the prior instance of the device to the new design, that the artifact of the 'limitation' of the holographic principle is due to the new device design, and yet there are a few desirable properties; which are that the base to emitter and collector to emitter pathways being linearized, and with this the impedance matching condition so actively.

There remain a few doubts that it is actively impedance matching the strict impedance relationship in direct current & alternating current, but as a consequence the data is explainable as not sensing two touches in the current design.

However the older design did indeed expand the notion of the light field to rotate in the current to voltage relationship around one another for the sake of the external device circuitry, while the new device does not operate this way.

As a consequence the older device although being unreliable did indeed function properly such that as a consequence of placing no restriction on the 'two dimensional' nature of the signals and expanding the notion of the light field 'around' the complex current to voltage relationship, there was no limitation on the holographic principle for multiple presses; and this is in fact positive indication that it is indeed possible to sample multiple presses with this external device circuitry.

As a consequence a new device needs to be built; but the important clue is that it will indeed be possible to realize a quantum optical computer without the restriction that is singular presses by way of the holographic principle, and indeed that:

1.) The expansion of the notion of the light field due to external device circuitry is possible.

2.) The current to voltage relationship can rotate around the current to voltage relationship.

3.) The holographic principle is fully realizable for the measurement of multiple presses.

Preliminary Lemma I: *Only with separation of variables is a true holographic principle possible.*

Lemma Proof I: *Only with a complete separation of variables is a given true holographic principle possible; fully articulable and expressible; once a given decomposition of physical nature is made possible; by the given that is articulation of an inexpressibility of physical form; as otherwise no given is true; nor possible as a given as a consequence of the conditionality of reality and the expressibility of reality given.*

Instructions for Device Development:

1.) The proper encoding for time in the externalized software layer is that of reduction to sorting by created date; as for moment of residual of base congruency of modular relation for combinatoric factorial for one of either of zero or literal two; before either of zero or one alone as either one of two or three of date; character; number; as time pre-existent for that of physical hardware of machine; for that of software within a physical.

2.) Either of these inseparabilities are knowable as either for physical as a physical unitary base foundation, that of one singular ending of neither so knowable; for that of singular physical being; for an immomentary awareness of two either's, from before such as considerations of five for each plurality so expressed before as.

Development of Clock Hardware Structure:

1.) Hypothetical: Either of two before a third; by the means of four point relations; recalls no pointer alone.

2.) Hypothetical: Both of three as a third before four; by the means of one point relation; recalls only point.

3.) Hypothetical: Either of one of two or three is as four; by the one of two point relations; only as potential.

4.) Hypothetical: Neither exclusive remains of either two or three; as one; from before four therefore as one.

5.) Hypothetical: Two of three of one are then therefore of if as either before both; as empty of any such for.

Conclusion of Development of Clock Hardware Structure:

A.) Tertiary empty relation exists as either before both of one; of each such two knowns so as undefined yet also locable within relation of physically known hardware architecture by software layer depth relationship.

Morals:

1.) Without peace of means to know of an aside by one of by five there remains sacrifice; hence another so is.

2.) Extrapolation of three into two from one remaining from four out of five remains; so known by an other.

Means:

1.) That of the first consideration is that of the fourth; for that of decidability of either or; & remaining as two.

2.) That of the second consideration is that of the first; for that of determination of both or either; of only one.

3.) That of the third consideration of any such three of the second or of the third as first remains one therefore.

4.) That of the fourth consideration of each such one of the first, second, and third is zero remainder as one if.

Ends:

1.) Inclusion within exclusion of for return of either any such three open relations admits open exterior of two.

2.) Exclusion of either two of order for three under any such one closed relation admits exterior open relation.

3.) Discrimination of both inclusion of each of before or after as empty relation admits open exterior therefore.

4.) Discernment of either such exclusions therefore forms each such open relation admitting exterior relations.

5.) Knowable interior with limitation therefore exists as inclusion with exclusion a part and excluded of thirds.

Structure of Development:

A.) Given that of the replacement of inseparable seamless passing of free current and voltage relationships of hardware between such means as the solid and volumetric extension of four capacities of power in relation to that of either of these admits open interior of volumetric extension under closure for either closed exteriorly open relation of seamlessness of interfacing of free reductive isolation of circuit; for each power free relation.

B.) Replacement of enclosure of battery within closure admits free operation without terminus of exteriorly formed means; as either such open interior relation forms closure under replacement by either open ending.

C.) Given free open relation of power affinity ground terminus of freely floating relation of alternating or (&) direct current relation is transparently of full capacity to pass either of three ways by way of two direct paths.

D.) As a consequence the relation of open affinities fixes the entropic group freely as singular relations of fixed points of free midpoints of machine states in enclosure; for each such point of thermodynamics at equilibrium.

E.) Each such point of thermodynamics exists at equilibrium; for either of any such closed limits are mutually definable as open under relation of equivalence of thermodynamical variables under free exchange of definite. limit is of variance only as each such inclusive open relation of definitional open entropic limitation of groups of temperature, pressure, entropy, capacity, power, energy, or motion; as inertially free comutual equilibrium.

F.) As such limits so defined are open in relation interiorly and exteriorly; neither chemical nor machine state are capable of outpacing or delimiting the structure of any such unnaturalized even structure of open closure, interference, and retention of capacitative action is retained as whole within one open interior relation of each.

G.) Under capacitative action of motion of kinetic form as inertia or potential motion of inertial form there is each such open relation of indivisibility of free open and infinitely extensible free relation of open equilibrium.

My list of Electronics Objectives:

1.). Test Oscilloscope after Refreshing CPROM/CMOS Means:

A.) Check with DC switch and LED and Reproducibility of Result of Disconnection and Reconnection.

B.) Saturation beyond possibility exists for one step ahead; hence CMOS refreshable now as compatible.

2.). Address question as to All Required Parts (Contingent as third step before two to be completed today.)

Measures:
1.) There is no strict inequality nor equality for the interval of this device; hence precision inadequate.

2.) Must use relation of 'exterior' inequality of excess of interior error relation for interior of error bars.

3.). Check Circuitry Design for Mistakes and Asses Validity of Component Values: Principles:

A.) Approximate valuations of interior and exterior component values; as centerless harmonic union.

B.) Scale appropriate under relative valuation of interior folding of four for exterior union of relation.

Principle:
C.) Interior valuation of passive over active impedance is topologically globally and locally equivalent; for any such pathway structure of connectedness; any two such points; and any two such interior forms.

D:) Exception; There is no free-standing circuit; although circuit without connections exist; as singular.

4.) Write further designs on devices to be built of three in number; accomplishing one task today and step one.

Implication:

1.). Subtending the relation of current machine design is compatible with that of reversal for one step.

2.). Bringing to bear the third device design; questions remain without a second unto a fifth step to 1.

5.) It is therefore decidable that current design; however proper for steps ahead must be done without mistakes.

Determination:
A.). A similar 'statistical' principle suffices to and confirms that of current and future design rules.
B.). Implementation of this statistical and mathematical design process is written and confirmed.

Precision:
C.). Difference of interior relation exists for that of exterior iff each full exterior subtends each element.

Assessment:
D.). Current topology would remain closed with no such third element if wired differently as to step 2.

6.). Confirmability of proper current wiring and implementation is confirmed as the second step to the others.

Preliminary:

1.). Valid testability of design process is of a saturation of interior geometric expansion of light field.

7.). Practicality of device determination of properties is checked at a given three (1,2,3) properties as with each.

Finality:
1.0). Hardware construction and wiring of proper operation is equivalently ohmic and saturated.
2.0). Freedom of operation from step three is equivalently bipartite for step two; and freely null.
3.0). Each check with that of third or second in functional order of three ends & begins at zero & open.

8.). Conclusion: Either of any three steps is open for any of each such one beginning at preliminary endings. Hence: Any such furtherance of design by paper; that of machine design; or that of process is free.

9.). Open conclusiveness of non-endings is also therefore determinable and hence; avoidable for extensions.

10.). Open contact of bridge acts as re-traversal and is valid as that of free opening of electromagnetism; from within that of exterior enclosure of device(s); for that of end before means of routing of light moment timing.

Jacket Assembly:

First: The laser diodes with part number: 38-1007-ND: D6505I from US-Lasers fit the 1 mm fiber optic cable.

Second: The Fiber Optic Click

part number: 1471-1612-ND:MIKROE-1940 fits the 2.1 mm fiber optic cable.

The 1 mm fiber optic cable fits the Fiber Optic Cable Plug with part number: 516-2077-ND: HFBR-4516Z.

Therefore all connections can be made; with 1 mm intermediary and spliced (no jacket) clearly around 15 cm acrylic disc with a multiplicity of inputs with the question of the intended purpose being that of timing of event structures; therefore that of point point relations of congruity for 10 laser diodes and 8 transceivers; for an even 18 as 10*2=20+/-8=8/12+/-10=20 relations with two open interior relation loops coupled separately through filter box; of different configuration than at first considered; with one input and one output (2 diodes); of open relation to one (1) loop; for which we have electromagnetic decoupling of that of light from physical matter.

A set of 10 (ten) laser diodes are an equivalent 20 separable (dual channel) i/o of the MAX11300 by 10 channels; therefore the remaining 8 (eight) suffice to insure that separable channeling of a full bit-word is decomposable by (eight) 8 interior relations of one stack; for a disc; of potential (insured) interior splicing of control of one (1) i/o of voltage nature; and four alterior interconnections to four; with a common (ground); that of a high (power photodiode in high) a low (power photodiode out low) and level (light emitting diode in).

As a consequence it is the photodiode that must be spliced; to mate two B(C/E) - B(C/E) bases to each other seamlessly; as one transparent relation of balance to be found in exterior domain of entire impedance matching. This requires two by two open relations of (2 A/DC) and off this relation four (2 Lasers) of input and output as two (2) fibers with splicing of voltage carrying metal wires to from touchscreen with filter as one two loop.

The connections remaining by this advantage of design indicate by the number of parts remaining the completeness of design for which there are from the given 10 a full 8 remaining; leaving 8 and 8 to be managed by that of the full circuitry of one individual processing system; with 8 pin and 8 pin of part cable purchased as (16) full digital bits; to relate to either of by 8 US-Laser's diodes and 8 Fiber Optic Click parts; as transceiver and receiver/send by 8 unique switchable channels; 8 unique transceiver PWM channels; and 2 bimodal switches making a complete 8 within 8 of full optical transceiver control on that of modal light interference of BCE nature to BCE nature; and therefore switchability/store/address/erase/restore/input/output/reverse nature; on that of the separable touchscreen of identification of 2 bimodal control bits of coupling and reverse input switchability of passthrough to touchscreen and from control hardware as single two (2) light/photo diode i/o.

Remainder of 8 and 8 under two sets (that of Click and that of Laser) possess 24 i/o; for which with beginning and end of separable i/o there remain 2x2=4 from 24 i/o (accomplishing at light speed with exception of empty) logical universal gate for 20 remaining i/o of which for the 4 both were of side of PWM Click control; as two (2) remaining as 6x2=12+8x1=8=20 total per cable i/e for exclusively that of one missing connect for two (2); that of a remainder of (1) spare and substituted (1) PWM switch for photodiode (C/E); with that of 1 hardline full pass bandwidth circuit; and that of 1 (20 channel (12 i/o bit PWM + 8 bit Laser PWM)) assembly; for 20 contacts.

Summary of Properties:

20 channel i/o as separable 12 bit i/o of PWM + 4 control bits of (16x4 (2 empty relations) = 64 bit assembly language of mathematics instruction set) of which 8 bit i/o of PWM + 4 bit i/o of bimodal relation make 24 bit word length of i/o as cyclic 12 bit non-zero non-one = 4096 layer depth of qubit with 8 bit control set of 256 separable free (byte) language set operations of 16 permutations of a 4 layer set of non-zero non-one open relation for that of sequential signal averaging circuit for each of the above eight (8) control processes; each as two (bit) discriminations by 4096/256/16=1 math instruction set per total loop unique relation of 8 bit layer fold depth fully; 20 bit layer machine depth fully; 12 bit layer depth language instruction set fully as 20x parallelism.

Fiber and fiber as 20 meeting 32 with one exception (2 bits of i/o as 4) match as 16 meeting 32 with two ends. Fiber and fiber in as 2 to 12=4096 instruction set; fiber and fiber out as 2 to 8=256 byte word length math set. Fiber and fiber as 8x2 and 12x2 equals 40 cables of 1 m long; for 40; with interior 8 bit i/o on 12 bit i/o = 20. Fiber and fiber as (8+10)=28x2=56+8 ground and power PD/LD connects as 64 bit qubit/8 bit analog hybrid.

Computation time is therefore with (20 MHz @ 128 MB/s @ Parallel Byte @ Sequential) = 32 bit instruction run execution per clock rate of 4 GHz and 256 (64x4) byte output of 1 GB per 4 GHz with 20 parallel processes of byte layer depth; for a total computational processing power from 8 bit i/o input of 20 bit i/o + 12 bit i/o output; of a conversion rate of processing from digital to analog of (limitation) 4 GHz @ 128 MB/s @ Byte / 32 GOP/s.

32 billion operations per second yields: 12 i/ 8 o/ 20 i/o bit instruction runtime of internal 8+4 Byte program / instruction length = 2x12 bit length program (assembly) = 4096 i/o bit/qubit analog/digital layer depth @ of i/o program speed 128 MB/s of an effective runtime depth of 2x32 (per switches) 64 bit per Hz of Byte conversion to Byte i/o of 4 GHz to as 32 billion operations per second on 2x64 bit = 4096 bit layer depth parallel bit i/o operations; for an equivalent operation of (hardware limitation) of 128 MB/s i/o over 32 GOPS for an effective interior operation processing speed of 32 GOPS per 20 MHz = 640 KHz per 4096 Bytes = 16+16 = 32 GOP/s; and external speed of i/o of 128 MB/s for a 1 second program @ data capacity of 4096 Bytes x 1/8 time x Bytes.

Observations:

Execution time of i/o of 1 second at full data capacity 128 MB/s for full machine instruction depth of (4096) as (16 bit full i/o (2 Byte)); sequentialized into 64 MB output from (4096) bit or 32 GHz per 64 MB Operations/s.

Interior data capacity: 4096 bit Exterior read off speed: 128 MB/s Internal processing speed: 32 GOP/s. Clock: 20 MHz

Input/Output Data Bus Limit: 64 MB per 128 MB @ 20 MHz Clock Rate.
I/O Processing Equivalence: 20 MHz @ 64 MB : 32 GOP/s @ 128 MB Instruction.
Operation Throughput: 24 bit : 4096 value @ 32 GOP/s @ 128 MB Instruction.
Operation Speed: 480 GB per 32 GOP/s as 1.5 seconds per 128 MB Instruction.
Correlation Exponent: 20!/(20-12)!(20-8)!)= 127,970 Simultaneous Parallel Operations. (128 KHz Fidelity)

Steps:

0.) There are two switches for separability of input and output on and off; either way through the circuit.

1.) The two of photodiode input and output need to be paralleled by each of the given parallels and photonic intermediary tangent space of separability of that of a mutual coparallel floating back to back register between the acrylic disc with fiber optics; and the signal averaging circuit; which has four input and output's of six; with two open interior connections for channeling of gain to gain ratio of apportionment of input to output as:

A: B(C/E) B: B(C/E)

2.) To be coupled to PWM as light current of one side of the relation being the two of (A, B) in the frequency averager; and on the either remaining side of the relation being the two of (PDI, PDO) with conversion from the (interior) of two T junctions of photodiode into a total of six (6) from four conversions of analog to light.

This is sufficient as an intermediary step to test with one 'Click' device for the Laser Diodes.

July 13th, 2018:

It has been determined the AD8305 is an active log intercept control unit on what otherwise would be as a given two separable amplitude controls on the variance of an AD6172 as the required element of the ADA or analog device averager; for which there is a multiplicity of variances of waves; their impedance relationships; and light passages through which we obtain control over collimation of the phase and amplitude information in sets of two; and for which the offset is null limited; for which free passthrough integrates and differentiates pure harmonic information into subsets of which are in a multiplicity of fibrous network managements of order zero; and information capacity of order one; with reduction to null forcing and damping.

The AD8302 is therefore considered for incorporation into the ADA; and it's consequent circuit of which will provide for resolutional decomposition to set/subset/superset of the optical chamber; of which has a full 10 layers for information management and sequentialization.

This offers a nice, quaint, and careful application of analog to digital crossover without distortion and active feedback resonance; the differing question here being as to a channel and configurational T retracing for that of either what is the forefront question (that of feedback to the main central touchscreen plat; or to that of it's separable input only optioned outcome.)

Decisions:

1.) 8305 NDZ to Canada Proto Advantage

2.) Two-Four more Photodiode / Light Emitting Diode

3.) Update and get Vishay Photoreceiver

Trick: Fishing line around cleaved optical cable along the long.

This affords for:

128 KHz parallel to series operations (conversions)
128 MB x 2 x 2 (4096) Memory in the process (tracking of 16536 points of inclusion in dataset).

Processing Speed:

20 MHz x 128 KHz = 2,560 G-Bit
320 (Giga) Flops